Reference Clock Frequency 1000 Mhz

Example synthesis of 734.3133739 Mhz, with 12 bit math/delay

Increment value = (2^12 *1000MHz/734.3133739MHz) - 2^12

Increment Value = 1482

Falling Edge Accumulator Start Value = (50% of (1000MHz/734.3133739MHz)*2^12)= 2789

TABLE 1

Rising Edge					Falling Edge				
Accumulator	Overflow bits	Base Accumulator	Equivalent Delay from Nearest Ref Edge (deg)	Total Effective Delay (deg)	Accumulator	Overflow bits	Base Accumulator	Equivalent Delay from Nearest Ref Edge (deg)	Total Effective Delay (deg)
0	0	0	0	0	2789	0	2789	245.13	245.13
1482	0	1482	130.25	490.25	4271	1	175	15.38	735.38
2964	0	2964	260.51	980.51	1657	0	1657	145.63	1225.63
4446	1	350	30.76	1470.76	3139	0	3139	275.89	1715.89
1832	0	1832	161.02	1961.02	4621	1	525	46.14	2206.14
3314	0	3314	291.27	2451.27	2007	0	2007	176.4	2696.4
4796	1	700	61.52	2941.52	3489	0	3489	306.65	3186.65
2182	0	2182	191.78	3431.78	4971	1	875	76.9	3676.9
3664	0	3664	322.03	3922.03	2357	0	2357	207.16	4167.16
5146	1	1050	92.29	4412.29	3839	0	3839	337.41	4657.41
2532	0	2532	222.54	4902.54	5321	1	1225	107.67	5147.67
4014	0	4014	352.79	5392.79	2707	0	2707	237.92	5637.92
5496	1	1400	123.05	5883.05	4189	1	93	8.17	6128.17
2882	0	2882	253.3	6373.3	1575	0	1575	138.43	6618.43
4364	1	268	23.55	6863.55	3057	0	3057	268.68	7108.68
1750	0	1750	153.81	7353.81	4539	1	443	38.94	7598.94
3232	0	3232	284.06	7844.06	1925	0	1925	169.19	8089.19
4714	1	618	54.32	8334.32	3407	0	3407	299.44	8579.44
2100	0	2100	184.57	8824.57	4889	1	793	69.7	9069.7
3582	0	3582	314.82	9314.82	2275	0	2275	199.95	9559.95
5064	1	968	85.08	9805.08	3757	0	3757	330.21	10050.21
2450	0	2450	215.33	10295.33	5239	1	1143	100.46	10540.46
3932	0	3932	345.59	10785.59	2625	0	2625	230.71	11030.71
5414	1	1318	115.84	11275.84	4107	1	11	0.97	11520.97
2800	0	2800	246.09	11766.09	1493	0	1493	131.22	12011.22
4282	1	186	16.35	12256.35	2975	0	2975	261.47	12501.47
1668	0	1668	146.6	12746.6	4457	1	361	31.73	12991.73